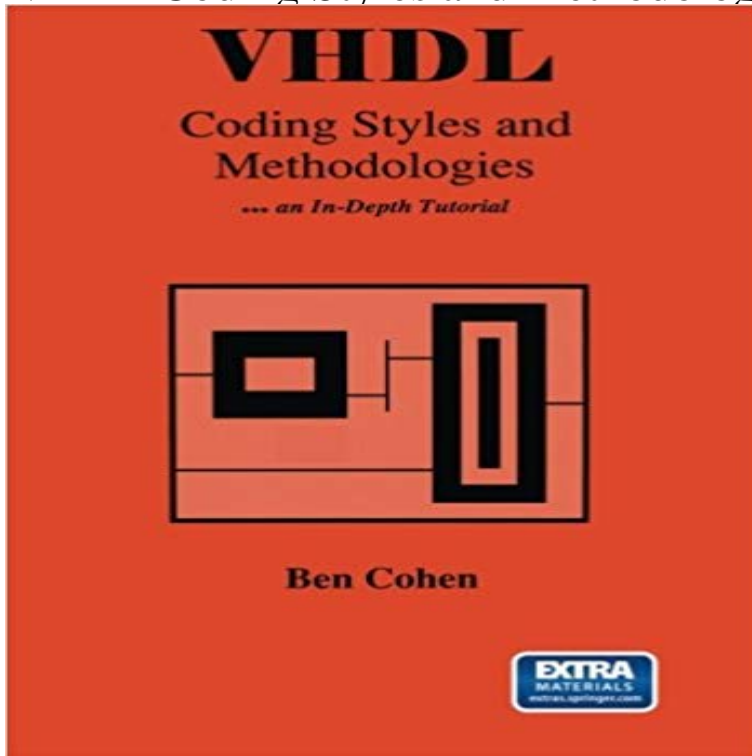


VHDL Coding Styles and Methodologies



VHDL Coding Styles and Methodologies was originally written as a teaching tool for a VHDL training course. The author began writing the book because he could not find a practical and easy to read book that gave in depth coverage of both, the language and coding methodologies. This book is intended for: 1. College students. It is organized in 13 chapters, each covering a separate aspect of the language, with complete examples. All VHDL code described in the book is on a companion 3.5 PC disk. Students can compile and simulate the examples to get a greater understanding of the language. Each chapter includes a series of exercises to reinforce the concepts. 2. Engineers. It is written by an aerospace engineer who has 26 years of hardware, software, computer architecture and simulation experience. It covers practical applications of VHDL with coding styles and methodologies that represent what is current in the industry. VHDL synthesizable constructs are identified. Guidelines for testbench designs are provided. Also included is a project for the design of a synthesizable Universal Asynchronous Receiver Transmitter (UART), and a testbench to verify proper operation of the UART in a realistic environment, with CPU interfaces and transmission line jitter. An introduction to VHDL Initiative Toward ASIC Libraries (VITAL) is also provided. The book emphasizes VHDL 1987 standard but provides guidelines for features implemented in VHDL 1993.

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